

**IN THE CLAIMS**

This listing of the claim will replace all prior versions and listings of claim in the present application.

**Listing of Claims**

Claims 1-6 (canceled)

7. (previously presented) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate ; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate.

8. (previously presented) A semiconductor multi-chip module according to claim 7, wherein said substrate is a multilayer wiring substrate.

9. (previously presented) A semiconductor multi-chip module according to claim 8, wherein said multilayer wiring substrate is a ceramic substrate.

10. (previously presented) A semiconductor multi-chip module according to claim 7, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

11. (previously presented) A semiconductor multi-chip module according to claim 7, wherein a checking function is provided for detecting faults in said semiconductor chips.

12. (previously presented) A semiconductor multi-chip module according to claim 11, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

13. (previously presented) A semiconductor multi-chip module according to claim 7, wherein at least one of said semiconductor chips is a memory for storing data.

14. (previously presented) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate,

wherein said first data lines correspond to a portion of a plurality of bits of a data signal formed by a portion of said data lines and said second data lines correspond to another portion of the bits of the data signal formed by another portion of said data lines.

15. (previously presented) A semiconductor multi-chip module according to claim 14, wherein said substrate is a multilayer wiring substrate.

16. (previously presented) A semiconductor multi-chip module according to claim 15, wherein said multilayer wiring substrate is a ceramic substrate.

17. (previously presented) A semiconductor multi-chip module according to claim 14, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

18. (previously presented) A semiconductor multi-chip module according to claim 14, wherein a checking function is provided for detecting faults in said semiconductor chips.

19. (previously presented) A semiconductor multi-chip module according to claim 18, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor when faults of said processor are detected.

20. (previously presented) A semiconductor multi-chip module according to claim 14, wherein at least one of said semiconductor chips is a memory for storing data.

21. (previously presented) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected

to said second data lines provided exclusively on said another side of said substrate,

wherein said first data lines corresponding to upper bits of said data lines and said second data lines corresponding to lower bits of said data lines.

22. (previously presented) A semiconductor multi-chip module according to claim 21, wherein said substrate is a multilayer wiring substrate.

23. (previously presented) A semiconductor multi-chip module according to claim 22, wherein said multilayer wiring substrate is a ceramic substrate.

24. (previously presented) A semiconductor multi-chip module according to claim 21, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

25. (previously presented) A semiconductor multi-chip module according to claim 21, wherein a checking function is provided for detecting faults in said semiconductor chips.

26. (previously presented) A semiconductor multi-chip module according to claim 25, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said when faults of said processor are detected.

27. (previously presented) A semiconductor multi-chip module according to claim 21, wherein at least one of said semiconductor chips is a memory for storing data.

28. (previously presented) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate ; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate.

29. (previously presented) A semiconductor multi-chip module according to claim 28, wherein said substrate is a multilayer wiring substrate.

30. (previously presented) A semiconductor multi-chip module according to claim 29, wherein said multilayer wiring substrate is a ceramic substrate.

31. (previously presented) A semiconductor multi-chip module according to claim 28, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

32. (previously presented) A semiconductor multi-chip module according to claim 28, wherein a checking function is provided for detecting faults in said semiconductor chips.

33. (previously presented) A semiconductor multi-chip module according to claim 32, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

34. (previously presented) A semiconductor multi-chip module according to claim 28, wherein at least one of said semiconductor chips is a memory for storing data.

35. (previously presented) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines

provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein said first data lines correspond to a portion of a plurality of bits of a data signal formed by a portion of said data lines and said second data lines correspond to another portion of the bits of the data signal formed by another portion of said data lines.

36. (previously presented) A semiconductor multi-chip module according to claim 35, wherein said substrate is a multilayer wiring substrate.

37. (previously presented) A semiconductor multi-chip module according to claim 36, wherein said multilayer wiring substrate is a ceramic substrate.

38. (previously presented) A semiconductor multi-chip module according to claim 35, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

39. (previously presented) A semiconductor multi-chip module according to claim 35, wherein a checking function is provided for detecting faults in said semiconductor chips.

40. (previously presented) A semiconductor multi-chip module according to claim 39, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

41. (previously presented) A semiconductor multi-chip module according to claim 35, wherein at least one of said semiconductor chips is a memory for storing data.

42. (previously presented) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein said first data lines corresponding to upper bits of said data lines and said second data lines corresponding to lower bits of said data lines.

43. (previously presented) A semiconductor multi-chip module according to claim 42, wherein said substrate is a multilayer wiring substrate.

44. (previously presented) A semiconductor multi-chip module according to claim 43, wherein said multilayer wiring substrate is a ceramic substrate.

45. (previously presented) A semiconductor multi-chip module according to claim 42, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

46. (previously presented) A semiconductor multi-chip module according to claim 42, wherein a checking function is provided for detecting faults in said semiconductor chips.

47. (previously presented) A semiconductor multi-chip module according to claim 46, wherein said semiconductor chips includes a processor

and the checking function is a watch dog timer for resetting said when faults of said processor are detected.

48. (previously presented) A semiconductor multi-chip module according to claim 42, wherein at least one of said semiconductor chips is a memory for storing data.

49. (new) A semiconductor multi-chip module, comprising:  
a substrate;

a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate ; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate,

wherein connection is made to said first data lines exclusively on said one side and connection is made to said second data lines exclusively on said another side.

50. (new) A semiconductor multi-chip module according to claim 49, wherein said substrate is a multilayer wiring substrate.

51. (new) A semiconductor multi-chip module according to claim 50, wherein said multilayer wiring substrate is a ceramic substrate.

52. (new) A semiconductor multi-chip module according to claim 49, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

53. (new) A semiconductor multi-chip module according to claim 49, wherein a checking function is provided for detecting faults in said semiconductor chips.

54. (new) A semiconductor multi-chip module according to claim 53, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

55. (new) A semiconductor multi-chip module according to claim 49, wherein at least one of said semiconductor chips is a memory for storing data.

56. (new) A semiconductor multi-chip module, comprising:  
a substrate;  
a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate,

wherein said first data lines correspond to a portion of a plurality of bits of a data signal formed by a portion of said data lines and said second data lines correspond to another portion of the bits of the data signal formed by another portion of said data lines, and

wherein connection is made to said first data lines exclusively on said one side and connection is made to said second data lines exclusively on said another side.

57. (new) A semiconductor multi-chip module according to claim 56, wherein said substrate is a multilayer wiring substrate.

58. (new) A semiconductor multi-chip module according to claim 57, wherein said multilayer wiring substrate is a ceramic substrate.

59. (new) A semiconductor multi-chip module according to claim 56, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

60. (new) A semiconductor multi-chip module according to claim 56, wherein a checking function is provided for detecting faults in said semiconductor chips.

61. (new) A semiconductor multi-chip module according to claim 60, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor when faults of said processor are detected.

62. (new) A semiconductor multi-chip module according to claim 56, wherein at least one of said semiconductor chips is a memory for storing data.

63. (new) A semiconductor multi-chip module, comprising:  
a substrate;  
a plurality of data lines including first data lines provided exclusively on one side of said substrate and second data lines provided exclusively on another side of said substrate;  
a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided exclusively on said one side of said substrate; and  
a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided exclusively on said another side of said substrate,

wherein said first data lines corresponding to upper bits of said data lines and said second data lines corresponding to lower bits of said data lines, and

wherein connection is made to said first data lines exclusively on said one side and connection is made to said second data lines exclusively on said another side.

64. (new) A semiconductor multi-chip module according to claim 63, wherein said substrate is a multilayer wiring substrate.

65. (new) A semiconductor multi-chip module according to claim 64, wherein said multilayer wiring substrate is a ceramic substrate.

66. (new) A semiconductor multi-chip module according to claim 63, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

67. (new) A semiconductor multi-chip module according to claim 63, wherein a checking function is provided for detecting faults in said semiconductor chips.

68. (new) A semiconductor multi-chip module according to claim 67, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said when faults of said processor are detected.

69. (new) A semiconductor multi-chip module according to claim 63, wherein at least one of said semiconductor chips is a memory for storing data.

70. (new) A semiconductor multi-chip module, comprising:

a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate ; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein connection is made to said first data lines on said one side of said substrate but not on another side of substrate and connection is made to said second data lines on said another side of said substrate but not on said one side of said substrate.

71. (new) A semiconductor multi-chip module according to claim 70, wherein said substrate is a multilayer wiring substrate.

72. (new) A semiconductor multi-chip module according to claim 71, wherein said multilayer wiring substrate is a ceramic substrate.

73. (new) A semiconductor multi-chip module according to claim 70, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

74. (new) A semiconductor multi-chip module according to claim 70, wherein a checking function is provided for detecting faults in said semiconductor chips.

75. (new) A semiconductor multi-chip module according to claim 74, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

76. (new) A semiconductor multi-chip module according to claim 70, wherein at least one of said semiconductor chips is a memory for storing data.

77. (new) A semiconductor multi-chip module, comprising:  
a substrate;  
a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein said first data lines correspond to a portion of a plurality of bits of a data signal formed by a portion of said data lines and said second data lines correspond to another portion of the bits of the data signal formed by another portion of said data lines, and

wherein connection is made to said first data lines on said one side of said substrate but not on another side of substrate and connection is made to said second data lines on said another side of said substrate but not on said one side of said substrate.

78. (new) A semiconductor multi-chip module according to claim 77, wherein said substrate is a multilayer wiring substrate.

79. (new) A semiconductor multi-chip module according to claim 78, wherein said multilayer wiring substrate is a ceramic substrate.

80. (new) A semiconductor multi-chip module according to claim 77, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

81. (new) A semiconductor multi-chip module according to claim 77, wherein a checking function is provided for detecting faults in said semiconductor chips.

82. (new) A semiconductor multi-chip module according to claim 81, wherein said semiconductor chips includes a processor and the checking function is a watch dog timer for resetting said processor chip when faults of said processor are detected.

83. (new) A semiconductor multi-chip module according to claim 77, wherein at least one of said semiconductor chips is a memory for storing data.

84. (new) A semiconductor multi-chip module, comprising:  
a substrate;

a plurality of data lines including first data lines provided on one side of said substrate but not on another side of substrate and second data lines provided on said another side of said substrate but not on said one side of said substrate;

a first group of semiconductor chips mounted on said one side of said substrate, said first group of semiconductor chips being connected to said first data lines provided on said one side of said substrate; and

a second group of semiconductor chips mounted on said another side of said substrate, said second group of semiconductor chips being connected to said second data lines provided on said another side of said substrate,

wherein said first data lines corresponding to upper bits of said data lines and said second data lines corresponding to lower bits of said data lines, and

wherein connection is made to said first data lines on said one side of said substrate but not on another side of substrate and connection is made to said second data lines on said another side of said substrate but not on said one side of said substrate.

85. (new) A semiconductor multi-chip module according to claim 84, wherein said substrate is a multilayer wiring substrate.

86. (new) A semiconductor multi-chip module according to claim 85, wherein said multilayer wiring substrate is a ceramic substrate.

87. (new) A semiconductor multi-chip module according to claim 84, wherein a semiconductor bare chip corresponding to each of said semiconductor chips is connected to said data lines by wire bonding.

88. (new) A semiconductor multi-chip module according to claim 84, wherein a checking function is provided for detecting faults in said semiconductor chips.

89. (new) A semiconductor multi-chip module according to claim 88, wherein said semiconductor chips includes a processor and the checking

function is a watch dog timer for resetting said when faults of said processor are detected.

90. (new) A semiconductor multi-chip module according to claim 84, wherein at least one of said semiconductor chips is a memory for storing data.